K016-CW43-Sw

IEEE802.11b/g/n Wireless LAN + Bluetooth 5.0

Combo Stamp Module

DATASHEET

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This specification may be changed with the improvement of the product. Please refer to the latest version of the usermanual.KERTONG TECHNOLOGY reserves the right of final interpretation and modification of all contents of this specification.

Revision History

Date	Revision Content	Revised By	Version
2018/04/26	- Preliminary	Qiu	1.0
2018/05/12	- Pin Definition Modified	Qiu	1.1
2018/05/27	- Bluetooth Spec Modified	Shawn	1.2
2018/06/12	- Add Process	Shawn	1.3
2018/12/25	- Add PCB Design Solder Paste definition	Liu	1.4
2019/01/03	- Delete FM feature	Liu	1.5
2019/01/21	- Add MSL Level / Storage Condition	Jason	1.6
2019/07/10	- Changed BT4.2 to BT5.0	Shawn	1.7
2020/01/06	- Add QDID and links	Shawn	1.8

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1. Introduction

1.1 About KERTONG

KERTONG Technologies Inc was established in Shenzhen in 2008. It is located in Baoan, Shenzhen. It is a high-tech enterprise specializing in the radio - related radio frequency series module application and the integrated solution platform of the products. At present, the product lines are: wireless network WIFI access module, wireless routing application module, wireless Bluetooth module, wireless Bluetooth box module, NFC communication module, GPS navigation module, Zigbee control module, wireless communication module and so on, as well as related module application solutions. The company has a complete set of 60 radio frequency integrated testers, 10 communication integrated testers, with a variety of wireless testing standards.

1.2 Product Overview

KERTONG Technologies to announce a low-cost and low-power consumption the combo module of K016-CW43-Sw model which has all of the WiFi(IEEE802.11b/g/n), Bluetooth (5.0) functionalities. And the highly integrated module makes the possibilities of web browsing Mini audio; Wireless projector; Bluetooth POS.ect and other applications. With seamless roaming capabilities and advanced security, also could interact with different vendors' 802.11b/g/n Access Points in the wireless LAN.

This K016-CW43-Sw module using the chipset from CYPRESS's the CYW43438 is advanced design techniques and process technology to reduce active and idle power, and designed to address the needs of highly mobile devices that require minimal power consumption and compact size. It includes a power management unit that simplifies the system power topology and allows for operation directly from a rechargeable mobile platform battery while maximizing battery life.

The K016-CW43-Sw module complies with IEEE 802.11 b/g/n standard and it can achieve up to a speed of 72.2Mbps with single stream in 802.11n draft, 54Mbps as specified in IEEE802.11g or 11Mbps for IEEE 802.11b to connect to the wireless LAN. The integrated module provides SDIO interface for WiFi, UART / I2S / PCM interface for Bluetooth.

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2. Features

- IEEE802.11b/g/n (WiFi/BT) single-band radio
- SDIO v2.0 host interface for WLAN and UP to 50MHz clock rate
- High speed UART and host interface for Bluetooth and Bluetooth UP to 4Mbps speed
- SZIE 12mm * 12mm * 1.5mm (L*W*H) LGA package

2.1 WLAN

- IEEE 802.11b/g/n single-band radio with an internal power amplifier, LNA, and T/R switch
- Simultaneous BT/WLAN reception with a single antenna
- ECI—enhanced coexistence support, which coordinates BT SCO transmissions around WLAN receptions
- WLAN host interface options:
  - ❒ SDIO v2.0, including default and high-speed timing.
  - ❒ gSPI—up to a 50 MHz clock rate
- Security:
  - ❒ WEP
  - ❒ WPA™ Personal
  - ❒ WPA2™ Personal
  - ❒ WMM
  - ❒ WMM-PS (U-APSD)
  - ❒ WMM-SA
  - ❒ WAPI
  - ❒ AES (Hardware Accelerator)
  - ❒ TKIP (host-computed)
  - ❒ WIFI Mode (apsta; ap ; p2p)

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2.2 Bluetooth

- Bluetooth v5.0 with integrated Class 1 PA
- Simultaneous BT/WLAN reception with a single antenna
- Concurrent Bluetooth, and WLAN operation
- HCI high-speed UART (H4 and H5) transport support
- BT UART (up to 4 Mbps) host digital interface that can be used concurrently with the above WLAN host interfaces.
- Bluetooth low power inquiry and page scan
- Bluetooth Low Energy (BLE) support
- Bluetooth Packet Loss Concealment (PLC)
- Bluetooth 2.1 + EDR
- Bluetooth 3.0
- Bluetooth 4.2
- Bluetooth 5.0 (Bluetooth Low Energy)
- BSA
- Mesh Internet (many to many)

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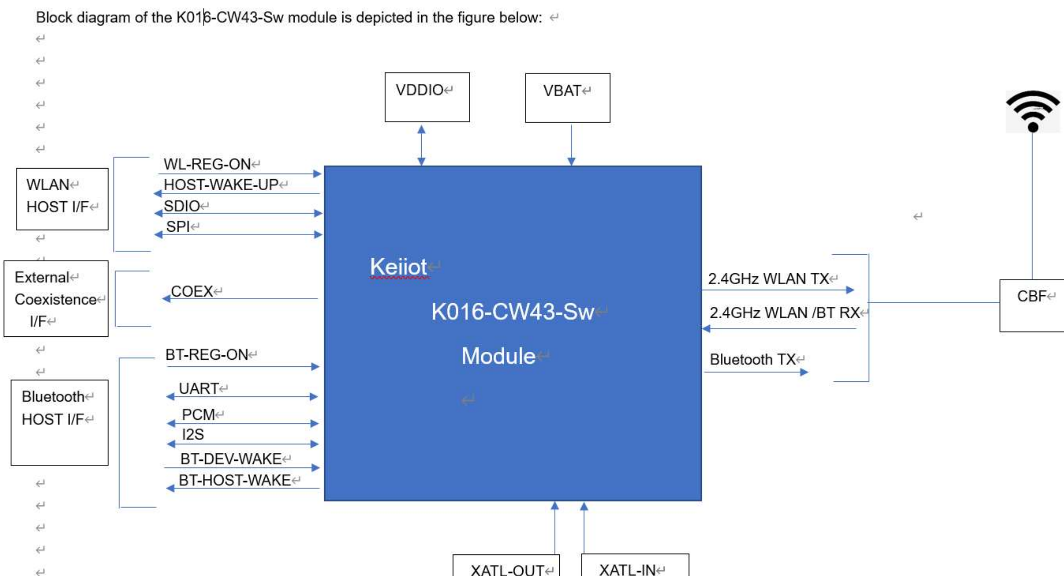
2.3 Block Diagram

A simplified block diagram of the K016-CW43-Sw module is depicted in the figure below:



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3. Specification Table

3.1 General Specification

Major Chipset	Cypress CYW43438
Model Name	K016-CW43-Sw
Product Description	Support WiFi/Bluetooth functionalities
Dimension	L x W x H: 12 x 12 x 1.5mm
WiFi Host Interface	SDIO v2.0
BT Interface	UART / PCM
Operating	-30°C to 85°C
Storage temperature	-40°C to 85°C
Humidity	Operating Humidity 10% to 95% Non-Condensing

3.2 Voltages (Absolute Maximum Ratings)

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	5.5	V
WL_VIO_SD	Digital/Bluetooth/SDIO/ I/O Voltage	-0.5	3.6	V

Results (2.4GHz)

Test Mode	DUT Status	Supply Voltage	Supply Voltage
		VBAT 3.3V	VDDIO3.3.V
802.11b 11Mbps	Continue TX	317.5mA	0.927mA
	Continue RX	57.8mA	0.879mA
802.11g 54Mbps	Continue TX	240.2mA	0.917mA
	Continue RX	57.8mA	0.879mA
802.11n MSC7	Continue TX HT20	231.9mA	0.903mA
	Continue RX HT20	57.8mA	0.879mA

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Requirement To measure the average current consumption in different working status.

Status		Supply Voltage VBAT 3.3V	Supply Voltage VDDIO3.3.V
ITEM	All OFF	2.2uA	488.7uA
WiFi	WiFi on mode	4.2mA	843.8uA
	WiFi scan mode	4.2mA	843.8uA
	WiFi Link mode	4.6mA	847uA
	RX throughput test(HT20)	83.8mA	843uA
	TX throughput test(HT20)	305mA	1mA
BT	BT ON	4.5mA	268.2uA
	BT scan mode	4.5mA	268.2uA
	BT pair with phone	4.5mA	268.2uA
	BT sleep mode	4.0uA	296.7uA
	FTP test	9.2mA	268.2uA

3.3 Recommended Operating Rating

	Min.	Typ.	Max.	Unit
Operating Temperature	-30	25	85	deg.C
VBAT	3.0	3.6	4.8	V
VDDIO	1.7	3.3	3.6	V

※NOTE: The K016-CW43-Sw module requires two power supplies: VBAT and VDDIO

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3.4 2.4GHz RF Specification

Feature	Description
WLAN Standard	IEEE 802.11b/g/n, WiFi compliant
Frequency Range	2.400 GHz ~ 2.497 GHz (2.4 GHz ISM Band)
Channels	2.4GHz：Ch1 ~ Ch13
Modulation	802.11b : DQPSK, DBPSK, CCK 802.11 g/n : OFDM /64-QAM,16-QAM, QPSK, BPSK
Output Power	802.11b /11Mbps : 16 dBm ± 1.5 dB @ EVM ≤ -9dB
	802.11g /54Mbps : 15 dBm ± 1.5 dB @ EVM ≤ -25dB
	802.11n /65Mbps : 14 dBm ± 1.5 dB @ EVM ≤ -28dB
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -85 dBm, typical
	- MCS=1 PER @ -84 dBm, typical
	- MCS=2 PER @ -82 dBm, typical
	- MCS=3 PER @ -80 dBm, typical
	- MCS=4 PER @ -77 dBm, typical
	- MCS=5 PER @ -73 dBm, typical
	- MCS=6 PER @ -71 dBm, typical
	- MCS=7 PER @ -68 dBm, typical
Receive Sensitivity (11g) @10% PER	- 6Mbps PER @ -86 dBm, typical
	- 9Mbps PER @ -85 dBm, typical
	- 12Mbps PER @ -85 dBm, typical
	- 18Mbps PER @ -83 dBm, typical
	- 24Mbps PER @ -81 dBm, typical
	- 36Mbps PER @ -78 dBm, typical
	- 48Mbps PER @ -73 dBm, typical
	- 54Mbps PER @ -71 dBm, typical
Receive Sensitivity (11b) @8% PER	- 1Mbps PER @ -90 dBm, typical
	- 2Mbps PER @ -88 dBm, typical
	- 5.5Mbps PER @ -87 dBm, typical
	- 11Mbps PER @ -84 dBm, typical
Data Rate	802.11b : 1, 2, 5.5, 11Mbps
	802.11g : 6, 9, 12, 18, 24, 36, 48, 54Mbps

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Data Rate (20MHz ,Long	802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps
Data Rate (20MHz ,short	802.11n : 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65,72.2Mbps
Maximum Input Level	802.11b : -10 dBm
	802.11g/n : -20 dBm
Antenna Re	Small antennas with 0~2 dBi peak gain

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3.5 Bluetooth Specification

Conditions : VBAT=3.6V ; VDDIO=3.3V ; Temp:25°C

Feature	Description		
Bluetooth Standard	Bluetooth V5. 0 and UP to 4 Mbps.		
QDID Number	134532		
Declaration ID	D043208		
Frequency Band	https://launchstudio.bluetooth.com/ListingDetails/89357 https://launchstudio.bluetooth.com/Listings/Search		
Host Interface	UART		
Antenna Reference	Small antennas with 0~2 dBi peak gain		
Frequency Band	2402MHz ~ 2480MHz	**Typical.**	**Max.**
Number of Channels	79 channels	8 dBm	
Modulation	FHSS, GFSK, DPSK, DQPSK	-86 dBm	
	Min.	-86 dBm	
Output Power (Class 1.5)		-80 dBm	
Sensitivity @ BER=0.1% for GFSK (1Mbps) Sensitivity @ BER=0.01% for π/4-DQPSK (2Mbps)	 GFSK (1Mbps):-20dBm		

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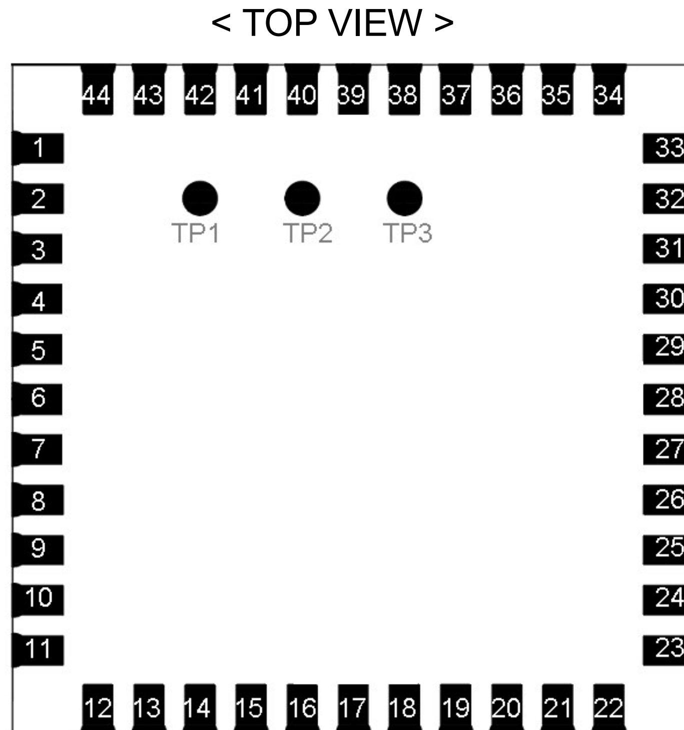
4. Pin Assignments

4.1 Pin Map



4.2 Pin Table

NO	Name	Type	Description
1	GND	—	Ground connections
2	WL_BT_ANT	I/O	WLAN/BT (RF->TX/RX) patch
3	GND	—	Ground
4	NC	—	Floating (Don't connected to ground)
5	NC	—	Floating (Don't connected to ground)
6	BT_WAKE	I	HOST wake-up Bluetooth device
7	BT_HOST_WAKE	O	Bluetooth device to wake-up HOST
8	NC	—	Floating (Don't connected to ground)
9	VBAT	P	Main power voltage source input
10	XTAL_IN	I	Crystal input
11	XTAL_OUT	O	Crystal output

12	WL_REG_ON	I	Internal regulators power enable/disable
13	WL_HOST_WAKE	O	WLAN to wake-up HOST
14	SDIO_DATA_2	I/O	SDIO data line 2
15	SDIO_DATA_3	I/O	SDIO data line 3
16	SDIO_DATA_CMD	I/O	SDIO command line
17	SDIO_DATA_CLK	I/O	SDIO clock line
18	SDIO_DATA_0	I/O	SDIO data line 0
19	SDIO_DATA_1	I/O	SDIO data line 1
20	GND	—	Ground connections
21	VIN_LDO_OUT	P	Internal Buck voltage generation pin
22	VDDIO	P	I/O Voltage supply input
23	VIN_LDO	P	Internal Buck voltage generation pin
24	LPO	I	External Low Power Clock input (32.768KHz)
25	PCM_OUT	O	PCM Data output
26	PCM_CLK	I/O	PCM clock
27	PCM_IN	I	PCM data input
28	PCM_SYNC	I/O	PCM sync signal
29	NC	—	Floating (Don’t connected to ground)
30	NC	—	Floating (Don’t connected to ground)
31	GND	—	Ground connections
32	NC	—	Floating (Don’t connected to ground)
33	GND	—	Ground connections
34	BT_RST_N	I	Low asserting reset for Bluetooth core
35	NC	—	Floating (Don’t connected to ground)
36	GND	—	Ground connections
37	GPIO4	I/O	WiFi Co-existence pin with LTE
38	GPIO3	I/O	WiFi Co-existence pin with LTE
39	GPIO2	I/O	WiFi Co-existence pin with LTE
40	GPIO1	I/O	WiFi Co-existence pin with LTE
41	UART_RTS_N	O	Bluetooth UART interface
42	UART_TXD	O	Bluetooth UART interface
43	UART_RXD	I	Bluetooth UART interface
44	UART_CTS_N	I	Bluetooth UART interface
45	TP1	O	NC
46	TP2	O	NC
47	TP3 (NC)	—	Floating (Don’t connected to ground)

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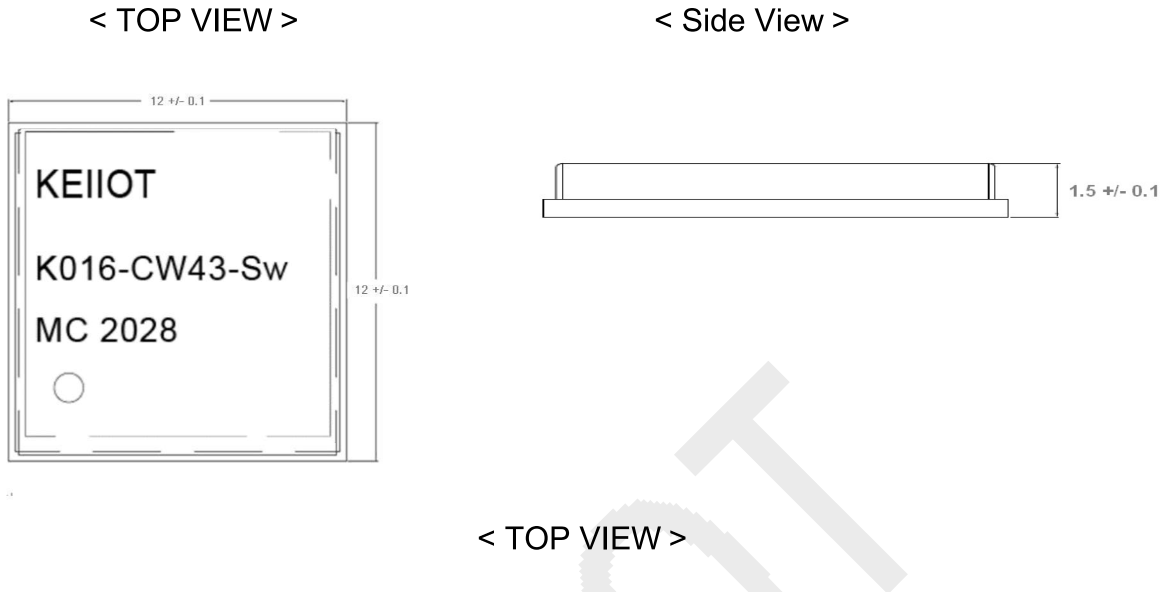
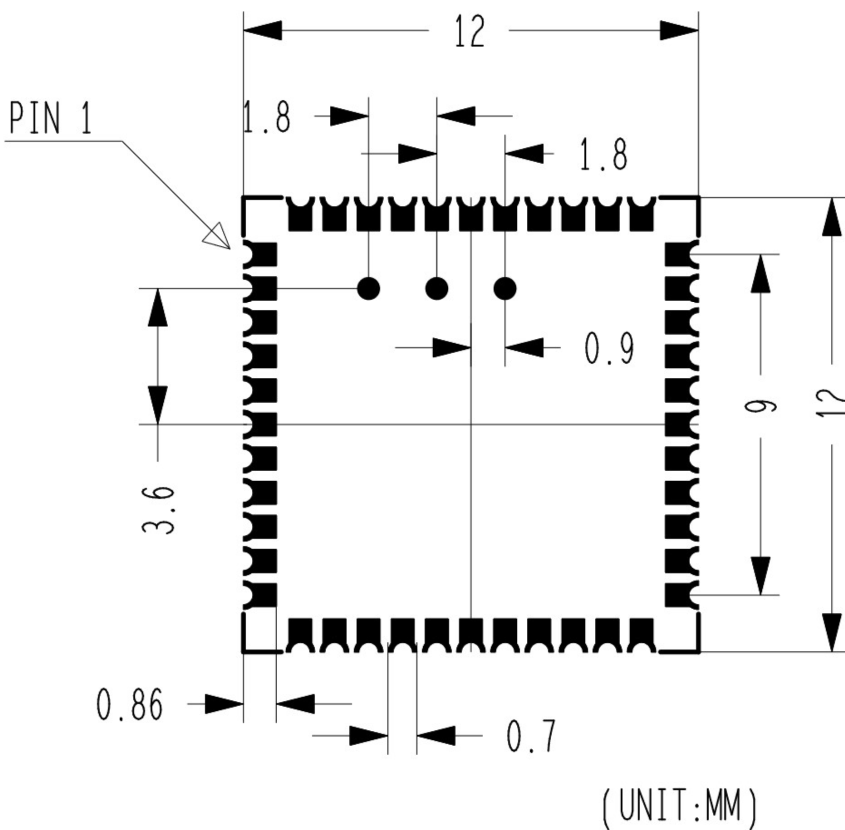
5. Mechanical and Layout Design

※NOTE (Unit:mm)

< TOP VIEW > < Side View >



< TOP VIEW >



6. Frequency References

6.1 External Clock Reference

The module uses a secondary low-frequency sleep clock for low-power mode timing. Either the internal low-precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz ± 30% over process, voltage, and temperature, which is adequate for some applications. However, one trade-off caused by this wide LPO tolerance is a small current consumption increase during power save mode that is incurred by the need to wake up earlier to avoid missing beacons.

External LPO signal characteristics:

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±30	ppm
Duty cycle	30 - 70	%
Input signal amplitude	400 to 1800	mV, p-p
Signal type	Square-wave or sine wave	-
Input impedance	>100k	Ω
	<5	pF
Clock jitter (integrated over 300Hz – 15KHz)	<10,000	ppm

External LPO signal characteristics:

1、ELECTRICAL SPECIFICATIONS

Hold Style	3225 Seam
Nominal Frequency	26.000000MHz
Mode	Fundamental / AT
Frequency Tolerance (at 25°C)	±10ppm
Frequency Stability Over Operating Temperature Characteristics	±10ppm
Operating Temperature Range	-20℃ ~ +70℃
Storage Temperature Range	-55℃ ~ +125℃
Shunt Capacitance (C_0)	5.0pF Max
Driver Level (Typical)	100μW
Load Capacitance(C_L)	12pF
ESR	60Ω Max
Insulation Resistance	More than 500Mohms at DC100V
Aging @25°C 1st year (Max)	±3ppm/year

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6.2 SDIO v2.0

The module supports SDIO version 2.0 for both 1-bit (25Mbps) and 4-bit (100Mbps),as well as high speed 4-bit (50 MHz clocks – 200 Mbps). Then has the ability to map the interrupt signal on a GPIO pin. This out-of-band interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force control of the gated clocks from within the WLAN chip is also provided.

Three functions are supported:

■ Function 0 standard SDIO function. The maximum block size is 32 bytes.

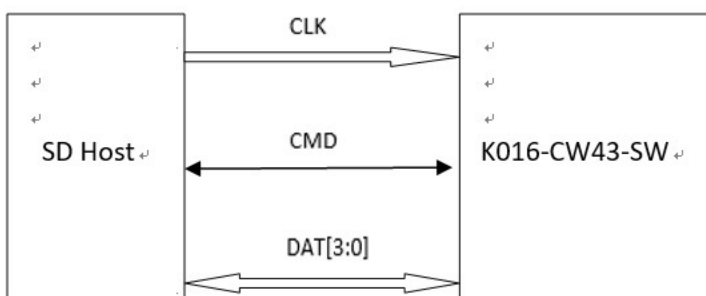
■ Function 1 backplane function to access the internal System-on-a-Chip (SoC) address space. The maximum block size is 64 bytes.

■ Function 2 WLAN function for efficient WLAN packet transfer through DMA. The maximum block size is 512 bytes.

SDIO PIN Descriptions

SD 4-Bit Mode	
DATA0	Data line 0
DATA1	Data line 1 or Interrupt
DATA2	Data line 2
DATA3	Data line 3
CLK	Clock
CMD	Command line

Signal Connections to SDIO Host



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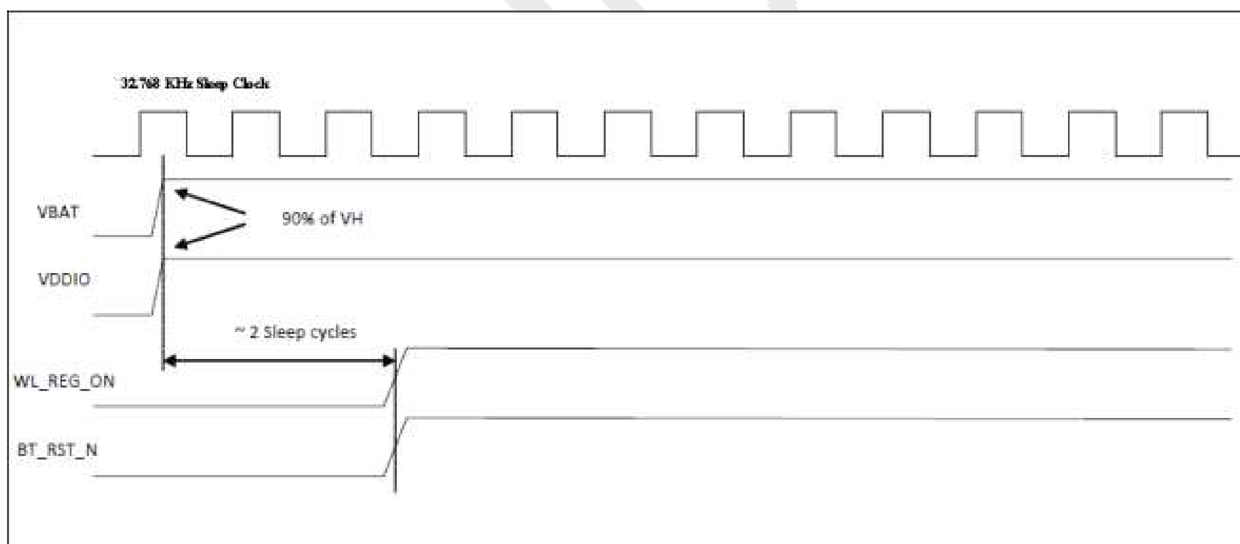
7. Interface Timing Diagram

7.1 Power-up Sequence Timing Diagram

The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.Additionally, diagrams are provided to indicate proper sequencing of the signals for carious operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

※ WL_REG_ON: Used by the PMU to power up the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.

※ BT_RST_N: Low asserting reset for Bluetooth only. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).



WLAN=ON, Bluetooth=ON

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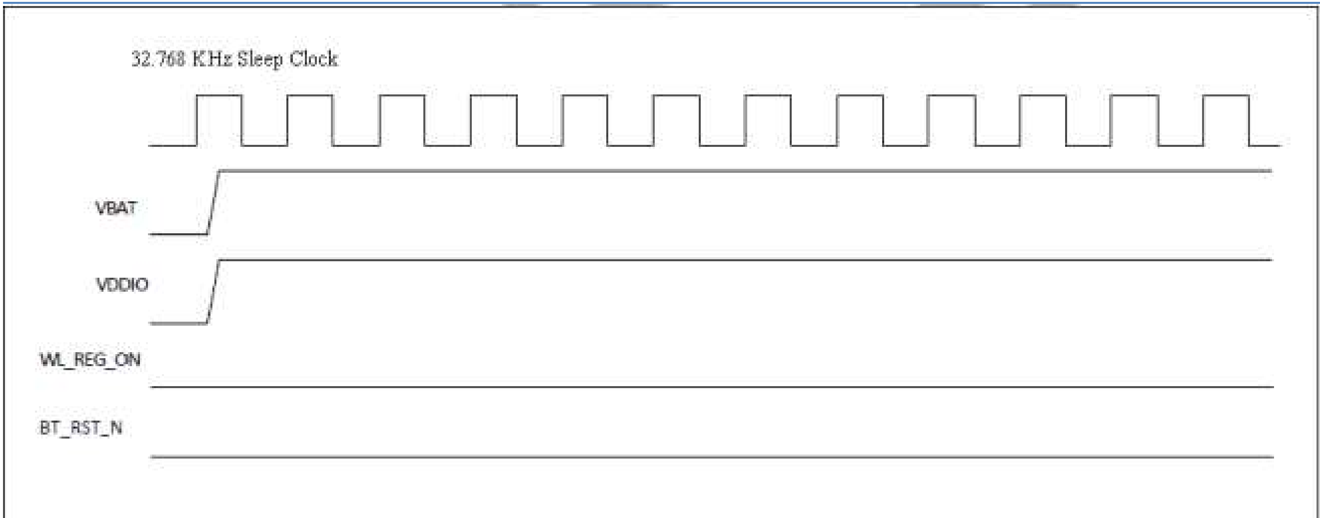
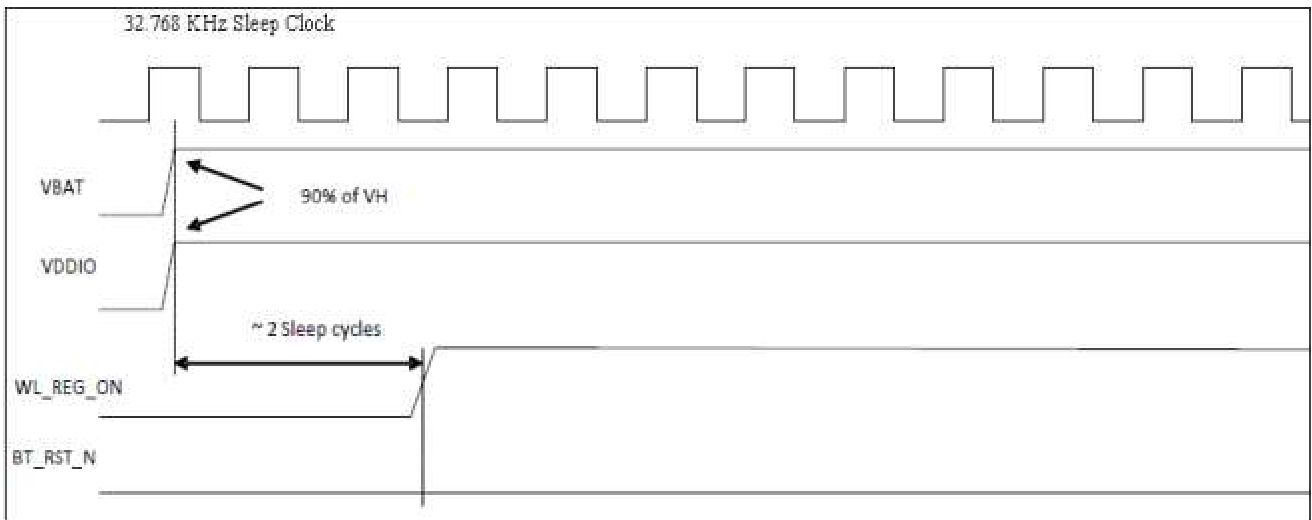
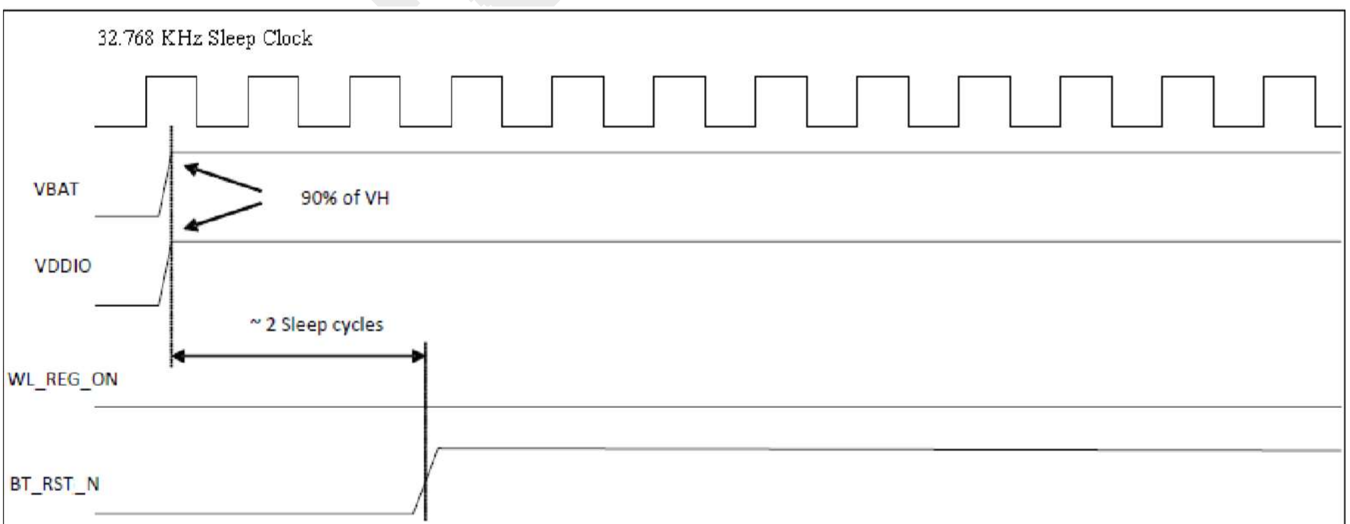


WLAN=OFF, Bluetooth=OFF

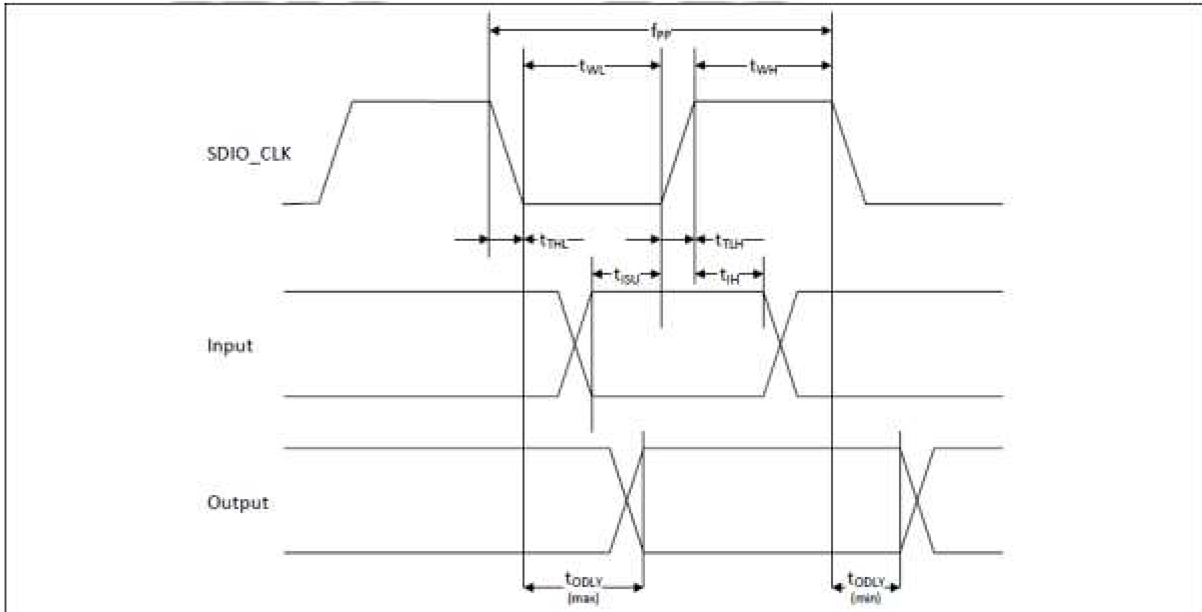


WLAN=ON, Bluetooth=OFF



WLAN=OFF, Bluetooth=ON

7.2 SDIO Default Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are refferred to minimum VIH and maximum VIL[b])					
Frequency-Data Transfer mode	fPP	0	-	25	MHz
Frequency-Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	10	-	-	ns
Clock high time	tWH	10	-	-	ns
Clock rise time	tTLH	-	-	10	ns
Clock low time	tTHL	-	-	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	-	-	ns
Input hold time	tIH	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	-	14	ns
Output delay time – Identification mode	tODLY	0	-	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data.

b. min(Vih) = 0.7 x VDDIO and max(Vil) = 0.2 x VDDIO.

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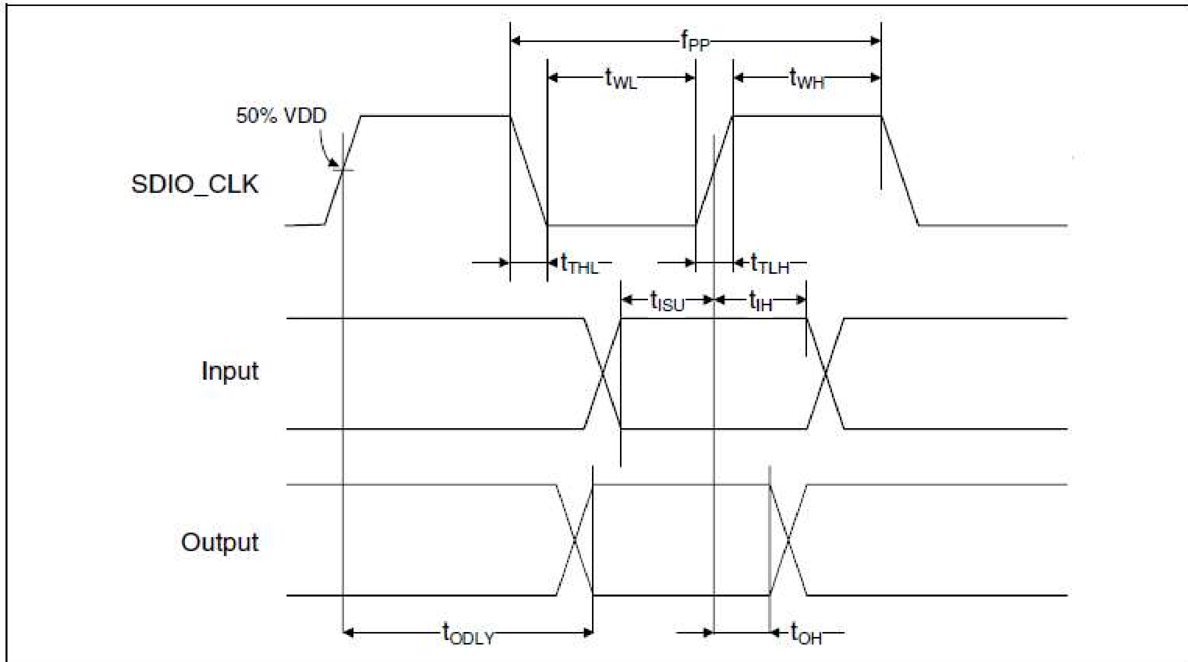
7.3 SDIO High Speed Mode Timing Diagram

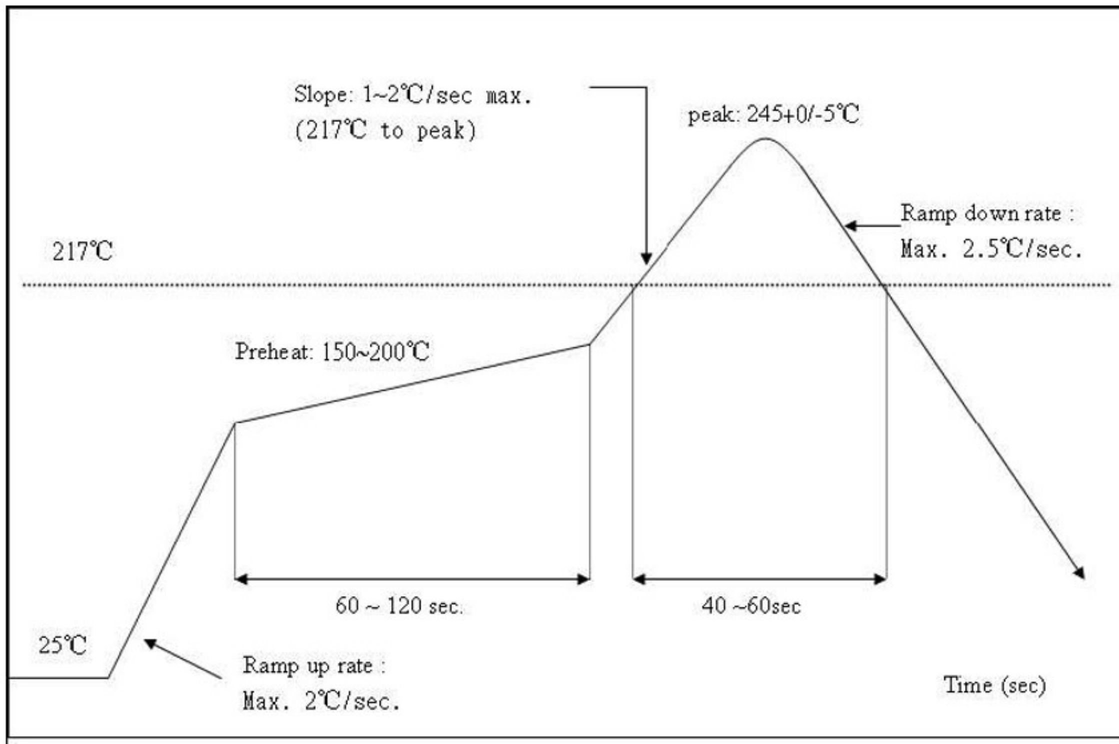


Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are refferred to minimum VIH and maximum VIL[b])					
Frequency-Data Transfer mode	fPP	0	-	50	MHz
Frequency-Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	7	-	-	ns
Clock high time	tWH	7	-	-	ns
Clock rise time	tTLH	-	-	3	ns
Clock low time	tTHL	-	-	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	6	-	-	ns
Input hold time	tIH	2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	-	-	14	ns
Output hold time	tOH	2.5	-	-	ns
Total system capacitance (each line)	CL	-	-	40	pF

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 x VDDIO and max(Vil) = 0.2 x VDDIO.

8. Recommended Reflow Profile

Referred to IPC/JEDEC standard.
Peak Temperature :<250°C Number
of Times : ≤2 times



ENVIRONMENTAL.

Operating :

※Operating Temperature: -10°C to +70 °C
※Relative Humidity: 5-90% (non-condensing)

Storage

※Temperature: -40°C to +80°C (non-operating)
※Relevant Humidity: 5-95% (non-condensing)

MTBF caculation

※Over 150,000hour

NOTE: it must use N2 for reflow and suggest the coneentration of oxygenless than 5000 ppm

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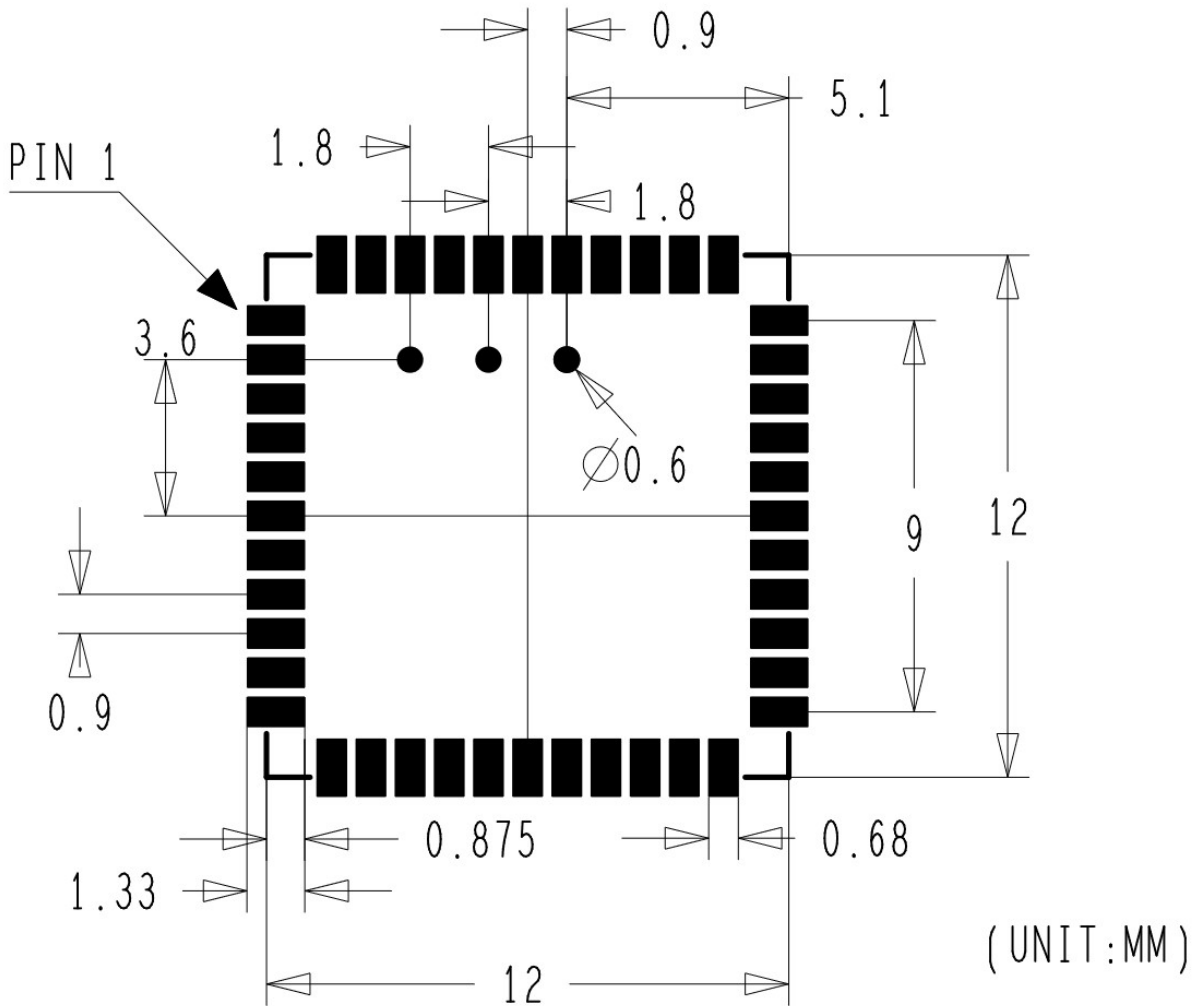
9. PCB Layout Solder Paste



- Module Specifications : W:0.65mm * L:0.95mm pitch 0.9 mm
- The proposed design W:0.65~0.75 mm * L:1.33mm. Consider not place other parts in the peripheral area of 1 mm ~ 1.5 mm to facilitate additional amount of solder for PCB pad.
- We Suggest the thickness of Stencil between 0.12 mm ~0.15mm, the W between 0.6~0.65mm and the L between L1.5~1.6mm.
- If the thickness of the stencil is thinner, we suggest to adding more solder, to increase the wetting ability. Depends on different production situation, if the stencil thickness is 0.08~0.1mm, and the module nearby area is no more space for expending soldering area, we will suggest to increase the stencil thickness to increase the wetting ability.
- The major consideration parts of stencil design is to increase the solder paste wetting ability.

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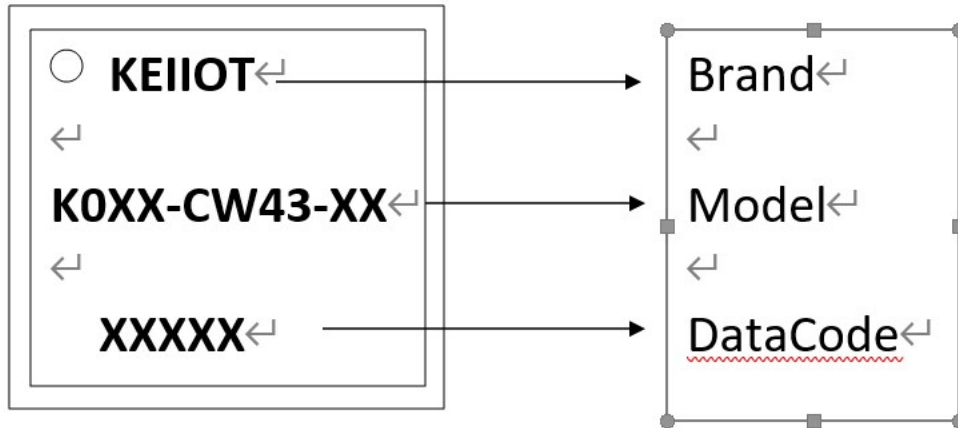
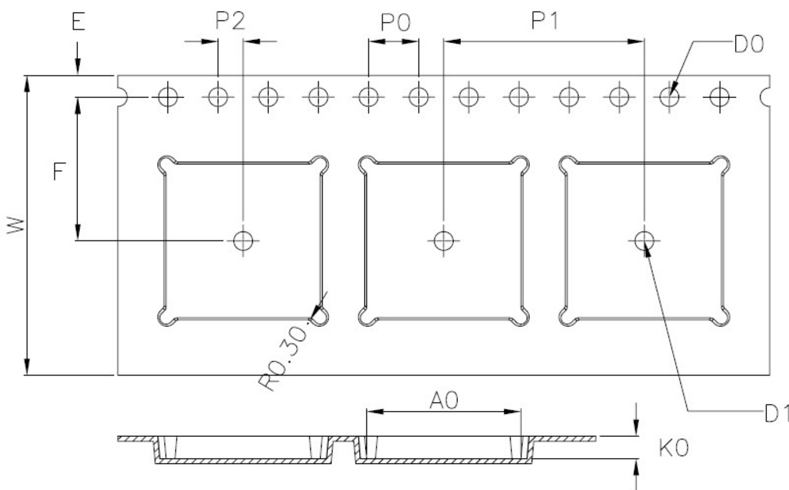
- Module Specifications L 0.7mm
- The design for PCB Pad : L:0.8mm
- We recommend the apertures for stencil L:0.5mm~0.6mm
- In order to avoid highness impact caused solder paste thickness, the stencil open size can be appropriately retracted

10. Package Information





W	24.00±0.30
A0	12.30±0.10
B0	12.30±0.10
K0	1.80±0.10
E	1.75±0.10
F	11.50±0.10
P0	4.00±0.10
P1	16.00±0.10
P2	2.00±0.10
D0	1.50 $^{+0.10}_{-0.00}$
D1	Ø1.50MIN

1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 22" reel : 98.5 Meters.(1:3)
7. Component load per 13" reel : 1500 pcs.

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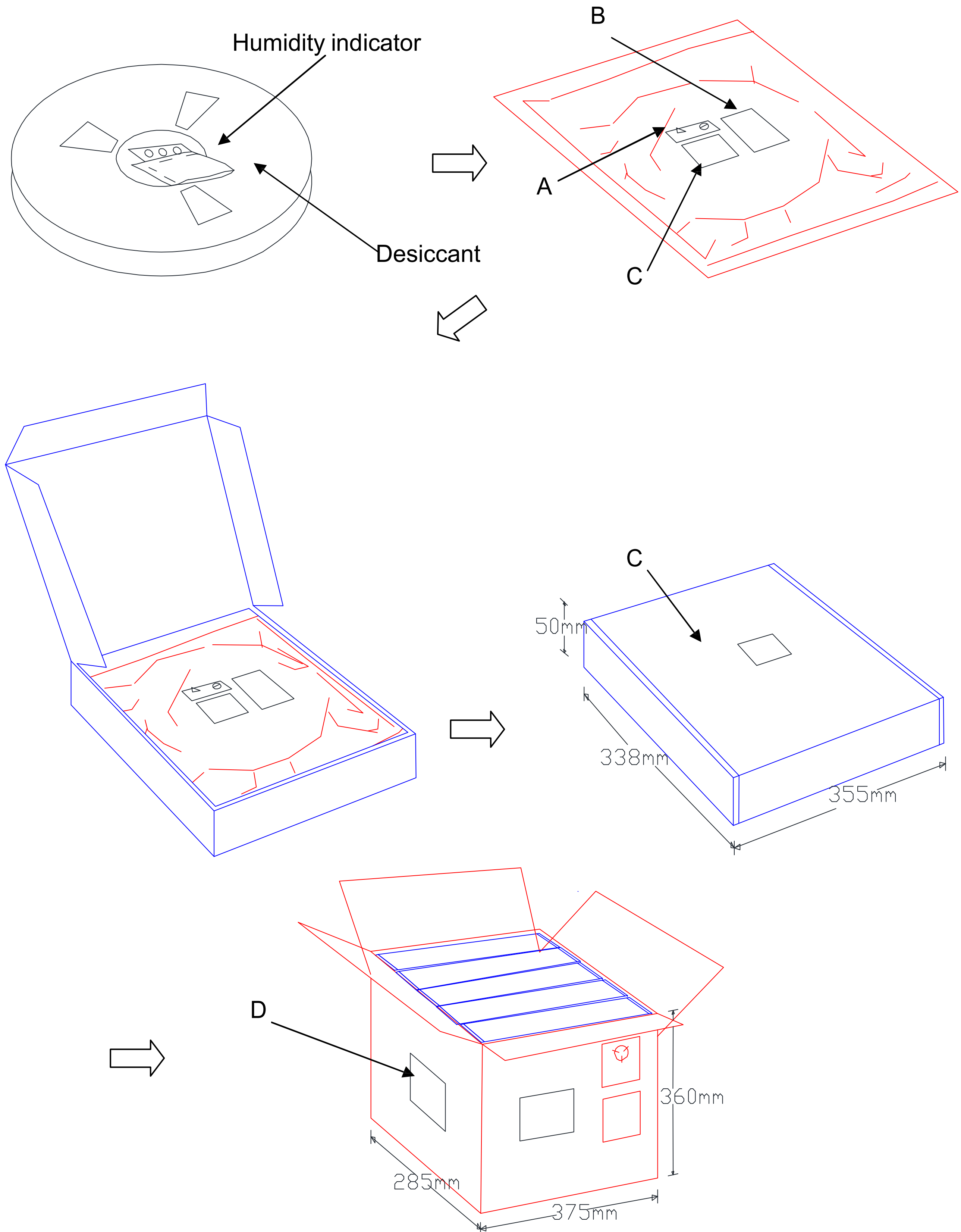
1> 1500pcs of per disc

2> 1500pcs * 5 =7500pcs (one Cartoon)



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11. This product is RoHS compliance

Wireless module before the SMT Note:

When customers Open stencil must be sure the hole bigger to the Wireless module plate, please press 1 to 1 and 0.7 mm is widened to open outward, the thickness of 0.12 mm.

① Can't get the wifi module bare hands when needs,must we wear the gloves and static ring.
The furnace temperature according to the size of the customer the mainboard ,generally like to stick on a tablet standard temperature of 250 + - 5,can do 260 + - 5. Storage and use Wifi module control should pay attention to the following matters:

① Module of the storage life of vacuum packaging：

1-1. Storage life： 12 months. Storage conditions:<40 . Relative ℃ humidity:<90%R.H.

1-2. 1-2.After this bag is opened , devices that will be subjected to infrared reflow, vapor-phase reflow, or equivalent processing must be

1-3. Check the humidity card :stored at ≦20%RH.If :30%~40%(pink)or greater than 40%(red).Labeling module has moisture absorption.

① Mounthed within 168 hours at factory conditions of: ≦ ℃t 30% ， ≦60%R.H.

② Once opened, the workshop the preservation of life for 168 hours.

1-4. If baking is required,devices may be baked for:

① Modules must be to remove module moisture problem.

② Baking temperature: 125 , 8 hours. ℃

③ After baking, put proper amount of desiccant to seal packages.

1-5. The actual number of module vacuum packing which is based on the actual number of packages to the customer requirements.

2. Module reel packaging items as follows.

2-1. Storage life： 12 months. Storage conditions:<40 . Relative ℃ humidity:<90%R.H.

2-2. Module apart packing after 168 hours，To launch patch need to bake, to remove the module hygroscopic, baking temperature conditions： 125℃，8hours.

2-3. The actual number of module reel packing which is based on the actual number of packages to the customer requirements.

3. Module pallet packaging items as follows：

3-1. Storage life： 3 months. Storage conditions:<40 . Relative ℃ humidity:<90%R.H.

3-2. Module if not used within 48 hours, before launch the need for baking, baking temperature: 125 , 8 hours. ℃

3-3. Pallet packaging each plate is 100 PCS.The actual number of module pallet packing which is based on the actual number of packages to the customer requirements.

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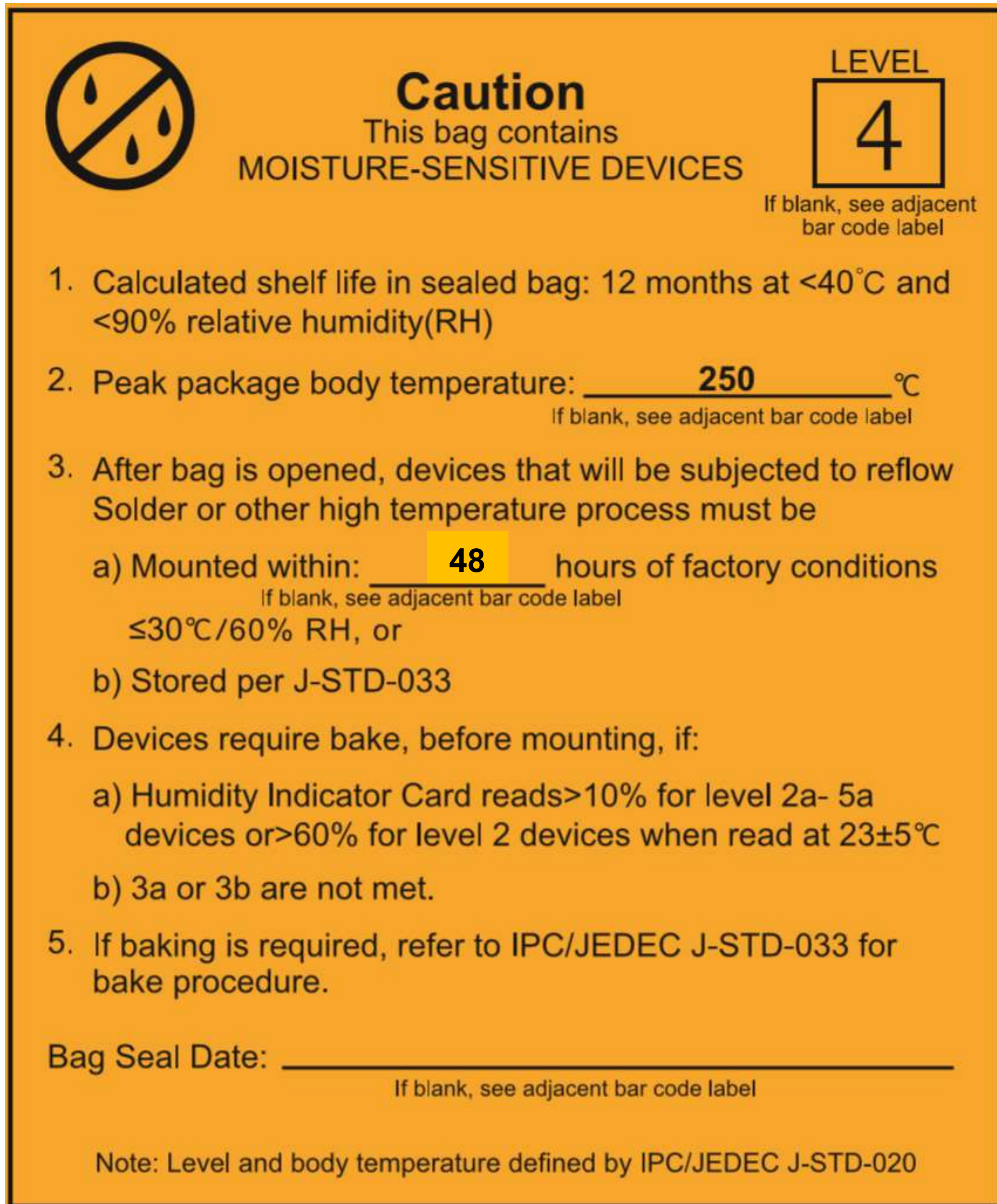
12. MSL Level / Storage Condition



※NOTE : Accumulated baking time should not exceed 96hrs